WHAT IS CLAIMED IS:

1. A display method characterized in that effective writing is conducted in a concentrated manner in a partial period during a frame period when a desired pixel value is written to a pixel in a hold-type display apparatus and, in so conducting, a write value in the partial period is set higher than the desired pixel value so that the desired pixel value is realized, in terms of visibility, by said writing in the partial period.

2. A display method characterized in that effective writing is conducted in a concentrated manner in a partial period during a frame period when a desired pixel value is written to a pixel in a hold-type display apparatus and, in so conducting, a predetermined relationship is given between an integral value of a write value written in the partial period and an integral value of the desired pixel value in the frame period.

3. A data write circuit, for driving a hold-type display apparatus, which includes means for performing effective writing in a concentrated manner in a partial period during a frame period when a desired pixel value is written to a pixel and which has means for setting a write value in the partial period higher than the desired pixel value so that

the desired pixel value is realized, in terms of visibility, by the writing in the partial period.

4. A data write circuit, for driving a hold-type display apparatus, which includes means for performing effective writing in a concentrated manner in a partial period during a frame period when a desired pixel value is written to a pixel and which has means for writing data in a manner such that a predetermined relationship is given between an integral value of a write value written in the partial period and an integral value of the desired pixel value in the frame period.

5. A data write circuit, for driving a hold-type display apparatus, which includes means for writing in a first period n times a desired pixel value to be written to a pixel and writing zero in a second period and thereafter where a frame period corresponding to a frame is divided into n parts and each divided period is denoted by first to *n*th period; n being an integer greater than or equal to 2.

6. A data write circuit according to Claim 5, wherein, when a pixel value that is n times the desired pixel value exceeds a displayable range of the display apparatus, said writing means writes to the pixel an upper limit value of the range in the first period, and an excess part that

remains unwritten is written to the pixel upon arrival of the second period and, thereafter, an excess part that cannot be written out in an *i*th period ($2 \leq i \leq n-1$) is written sequentially upon arrival of an (*i*+1)th period.

7. A data write circuit, for driving a hold-type display apparatus, which includes means for writing in an *i*th period ($2 \leq i < n$) n times a desired pixel value to be written to a pixel and writing zero in periods other than the *i*th period where a frame period corresponding to a frame is divided into n parts and each divided period is denoted by first to *n*th period; n being an integer greater than or equal to 2.

8. A data write circuit according to Claim 7, wherein, when a pixel value that is n times the desired pixel value exceeds a displayable range of the display apparatus, said writing means writes, in the *i*th period, an upper limit value of the range to the pixel and distributes an excess part that cannot be written out in a symmetrical manner with the *i*th period at a center, so that pixel values thus distributed before and after the *i*th period are written to the pixel.

9. A data write circuit according to Claim 5, including:

a counter which counts write clocks of n times a normal speed;

a memory control unit which reads out a pixel value from a frame memory based on an output from said counter;

an output value determining unit which determines whether the current period is one of first to *n*th periods, based on an output from said counter and which outputs a write value corresponding to the thus determined period; and

a plurality of switches which transmit the write values outputted from said output value determining unit to pixels corresponding thereto.

10. A data write circuit according to Claim 7, including:

a counter which counts write clocks of n times a normal speed;

a memory control unit which reads out a pixel value from a frame memory based on an output from said counter;

an output value determining unit which determines whether the current period is one of first to *n*th periods, based on an output from said counter and which outputs a write value corresponding to the thus determined period; and

a plurality of switches which transmit the write values outputted from said output value determining unit to pixels corresponding thereto.

11. A data write circuit according to Claim 9, further including a range compressing unit which compresses a range of the pixel, prior to determination by said output value

determining unit.

12. A data write circuit according to Claim 10, further including a range compressing unit which compresses a range of the pixel, prior to determination by said output value determining unit.

13. A data write circuit according to Claim 5, further including means for calculating a pixel value to be written to the pixel, at the time the pixel value is written in the first to *n*th periods, in a manner such that the pixel value is calculated after the frame is reconstructed by incorporating a motion compensation that corresponds to time shifts for the divided periods.

14. A data write circuit according to Claim 7, further including means for calculating a pixel value to be written to the pixel, at the time the pixel value is written in the first to *n*th periods, in a manner such that the pixel value is calculated after the frame is reconstructed by incorporating a motion compensation that corresponds to time shifts for the divided periods.

15. A data write circuit according to Claim 13, further including means for judging, based on the reliability of the reconstructed frame, whether calculation of a pixel value

utilizing the reconstructed frame is to be performed or not.

16. A data write circuit according to Claim 14, further including means for judging, based on the reliability of the reconstructed frame, whether calculation of a pixel value utilizing the reconstructed frame is to be performed or not.

17. A hold-type display apparatus, including:

a pixel array;

a data write circuit which writes data to said pixel array in a row direction and performs effective writing in a concentrate manner in a partial period during a frame period when a desired pixel value is written to a pixel and which has means for setting a write value in the partial period higher than the desired pixel value so that the desired pixel value is realized, in terms of visibility, by the writing in the partial period; and

a scanning line drive circuit which scans said pixel array in a column direction.

18. A hold-type display apparatus, including:

a pixel array;

a data write circuit which writes data to said pixel array in a row direction and performs effective writing in a concentrate manner in a partial period during a frame period when a desired pixel value is written to a pixel and which

has means for writing data in a manner such that a predetermined relationship is given between an integral value of a write value written in the partial period and an integral value of the desired pixel value in the frame period; and

a scanning line drive circuit which scans said pixel array in a column direction.

19. A hold-type display apparatus, including:

a pixel array;

a data write circuit, for writing data to said pixel array in a row direction, which includes means for writing in a first period n times a desired pixel value to be written to a pixel and writing 0 (zero) in a second period and thereafter where a frame period is divided into n parts and each divided period is denoted by first to nth period (n being an integer greater than or equal to 2); and

a scanning line drive circuit which scans said pixel array in a column direction.

20. A hold-type display apparatus, including:

a pixel array;

a data write circuit, for writing data to said pixel array in a row direction, which includes means for writing in an ith period ($2 \leq i < n$) n times a desired pixel value to be written to a pixel and writing zero in periods other than

the *i*th period where a frame period is divided into n parts and each divided period is denoted by first to *n*th period; n being an integer greater than or equal to 2; and

a scanning line drive circuit which scans said pixel array in a column direction.